What is claimed is:

1. A flip flop comprising:

a first switching element in which a first terminal thereof is connected with a data input terminal;

a first inverter element in which an input terminal thereof is connected with a second terminal of the first switching element;

a second switching element in which an output of the first inverter element is inputted to a first terminal thereof; and

a second inverter element in which an input terminal thereof is connected with a second terminal of the second switching element,

wherein an output terminal of the second inverter element is a data output terminal.

2. A flip flop according to claim 1; further comprising a first MOS transistor and a second MOS transistor,

wherein the output of the first inverter element is inputted to a gate terminal of the first MOS transistor and a drain of the first MOS transistor is connected with the input terminal of the first inverter element, and

wherein the output of the second inverter element is inputted to a gate terminal of the second MOS transistor and a drain of the second MOS transistor is connected with the input

terminal of the second inverter element.

3. A flip flop according to claim 2; wherein the first switching element is composed of a first NMOS transistor, a first control signal (CX) is inputted to a gate of the first NMOS transistor, the second switching element is composed of a second NMOS transistor, and a second control signal (C) is inputted to a gate of the second NMOS transistor.